IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	En-Hsing Chen et al.		
Title:	NAND MEMORY ARRAY INCORPORATING MULTIPLE SERIES SELECTION DEVICES AND METHOD FOR OPERATION OF SAME		
Application No.:	10/729,865	Filed:	December 5, 2003
Examiner:	Nguyen, Van Thu T.	Group Art Unit:	2824
Atty. Docket No.:	023-0029	Confirmation No.:	8494

November 13, 2007

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REPLY BRIEF (37 C.F.R. § 41.41)

This brief is in response to the Examiner's Answer, mailed September 12, 2007, which sets a period for reply ending November 13, 2007 (November 12 being a holiday in the District of Columbia). The fee, if any, is provided as directed in an electronic submission of this paper or in a transmittal letter accompanying this paper. Appellants respectfully request consideration of the following in connection with the present appeal.

Substantive arguments laid out in the Appeal Brief establish the legal error represented by the present Final Rejection. However, several aspects of the Examiner's Answer warrant comment.

RESPONSE TO ARGUMENT (paragraph 10)

Sub-paragraph I-a

The Examiner states that Tatsukawa "clearly shows DG2 is connected in series with SGS1, both DG2 and SGS1 are connected to the NAND string, and both DG2 and SGS1 are connected to the second end of the NAND string (see Fig. 8). Therefore, DG2 corresponds to a selection device at an end of the NAND string."

Moreover, the Examiner submits that the claim 1 language does not recite where the second end of the one NAND string exists with respect to the second selection device, and further suggests that there is no connectional relationship, "other than the second selection devices are simply 'include[d] ... at a second end.' "

This position ignores the language of the claim, which recites "said NAND strings *including* at a first end *thereof* a respective plurality of series selection devices of like type, wherein each NAND string *includes* a second plurality of series selection devices of like type at a second end *thereof*, ..." This is a clear textual reference to the selection devices being part of each NAND string. A dummy device that is not part of the NAND string cannot be viewed as a select device for the NAND string.

The Examiner reinforces Appellant's very argument with the statement "[a] NAND string often comprises a series of memory cells and select transistors connected *between* a sub-bit line and a sub-source line." (emphasis added) Applicant submits that the DG2 transistor may be connected to the same SL line *to which* the NAND string is connected, but such a transistor does not represent a select device of the NAND string as structurally recited in the claim.

Sub-paragraph I-b

The Examiner states that Tatsukawa "clearly discloses and shows DG2 is selectively activated by a control signal SD2 applied to its gate; and therefore, DG2 is seen as a selection device." Appellant notes that a *selectively activated* device is not necessarily a *selection* device. As an example, the memory cells in the NAND string are selectively activated devices, and yet do not represent selection devices.

The Examiner repeats both of these arguments in later sub-paragraphs. Each occurrence fails for the same reasons.

Sub-paragraph I-f

Appellant's comments in the Appeal Brief were in specific response to the arguments advanced by the Examiner in the Final Rejection, in support of the "conclusion" that the dummy

transistor "DG2 is seen as a selection device." Appellant maintains these comments as appropriate in response to the Examiner's earlier arguments.

Sub-paragraph I-g

Appellant maintains the argument, advanced in the Appeal Brief, that the Examiner is ignoring clear structural limitations recited in the claim, as described above with regards to sub-paragraph I-a.

Sub-paragraph II-a

The Examiner argues that "[one] of ordinary skill in the art at the time of the invention would most certainly understand that the series selection device of Tatsukawa inherently, or implicitly, has a charge storage dielectric." Appellant notes that Tatsukawa discloses floating gate memory cells, and says nothing about a charge storage dielectric. Inherency is a strict standard that requires that such must necessarily be the case, and not be a mere possibility. Appellant submits that such alleged inherency misunderstands the reference and/or the law. Moreover, the Examiner's unfounded inherency allegation is not understood here, as Sakui is cited for teaching such a dielectric.

CONCLUSION

For the at least the reasons outlined herein and in the Appellant's Brief, Appellants' presently claimed invention was not anticipated under 35 U.S.C. § 102(b) by the cited prior art, and would not have been obvious to one of ordinary skill in the art under 35 U.S.C. § 103(a) in view of the cited prior art. Accordingly, this honorable Board is respectfully requested to reverse the rejections and to direct the claims of the present application to be issued.

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Andrew C. Graham — 11-13-07 (Date)

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Respectfully submitted,

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